DESIGN AND PERFORMANCE ASSESSMENT OF A MULTIGIGABIT CLOCK-RECOVERY CIRCUIT

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ABSTRACT

This paper presents the design and experimental results of a nonlinear circuit and a tuned amplifier developed in the same GaAs monolithic microwave integrated circuit (MMIC), used in a 20 Gsymbol/s open-loop clock recovery unit. The nonlinearity is an unbalanced structure and its input stage performs the necessary signal formatting to reduce the recovered clock jitter, avoiding the use of additional pre-filtering. Both circuits were integrated in the same MMIC in order to improve the reliability, performance and to reduce the size and cost. Performance assessment of the clock recovery unit consisting of the two designed circuits and a high-Q bandpass filter is carried out, considering two different line codings, binary NRZ (20 Gbit/s) and 4-level (40 Gbit/s).

INTRODUCTION

The clock recovery function has long been recognised has one of the most critical receiver units (1). It is essential for any retimed receiver to have a high quality clock recovery unit (CRU). This provides a very precise local clock in order to perform accurately the regeneration and demultiplexing operations.

Clock recovery circuits can be classified into two groups: open-loop structures and closed-loop or adaptive structures. The former is usually built using a nonlinearity, which is necessary whenever the incoming signal lacks a discrete spectral line at the transmission rate, and a narrowband filter to recover this spectral line from the remain spectrum. The later approach makes use of the phase-lock principle and it may simply consist of a nonlinearity followed by a PLL. From a conceptual point of view the adaptive approach is preferable, since the phase-lock principle has inherent automatic frequency control (AFC) capabilities together with low bandwidths. Also this approach offers the potential of complete integration. However, at very high bit rates, the technology needed for a good design and performance of such circuits is not completely mature and the open-loop solution is preferable. The block diagram of an open-loop CRU is presented in Figure 1.

It includes a prefilter, a nonlinear circuit (NLC), a high quality factor (Q) bandpass filter and a tuned amplifier. The prefilter reshapes the incoming signal, in order to reduce the recovered clock jitter (2). A discrete frequency component at the data rate is generated using a nonlinear circuit. The high-Q bandpass filter reduces the noise level associated to the produced discrete component, and at the considered data rate it is implemented using a dielectric resonator (DR). Finally, the tuned amplifier has three main purposes: to provide the required signal levels, to reduce the degradation caused by the out of band spurious modes of the non-ideal high-Q bandpass filter and also to isolate the CRU from the subsequent units.

In the following sections we present the design and experimental results of a NLC and a tuned amplifier at 20 GHz, and evaluate the performance of the CRU consisting of the two implemented circuits, connected by a narrow bandpass filter (NBPF).

The two subsystems were designed on the same GaAs MMIC by using the D02AH process from PML (3). This process provides field effect transistors with high electronic mobility (HEMT) and reduced gate lengths (0.2 μm), thus enabling the production of low noise transistors (N_F=0.9 dB@12 GHz, with G_A=11.5 dB), with high transition frequency (F_T=62 GHz).

The design of the clock recovery subsystems was performed using the commercial microwave simulator HP-MDS (4).

NONLINEARITY AND AMPLIFIER DESIGN

The implemented NLC is an unbalanced nonlinearity, since such structure can be achieved with very simple circuits, and there is only negligible degradation in performance when compared to a balanced nonlinearity, as concluded by Matos *et al* (5). It was demonstrated from simulation study (5) that for raised cosine elementary pulses with moderate to high roll-off factors, the degradation in performance by using a truncated nonlinearity is negligible compared with the more common absolute value and full squarer nonlinearities.

An unbalanced nonlinearity can be accomplished by using simply a properly biased HEMT, as will be shown next. A GaAs FET drain to source current is approximated by (6):

$$I_{DS}=\begin{cases}\beta(V_{GS}-V_{TO})^2(1+\lambda V_{DS})\tanh(\alpha V_{DS}) & V_{GS}\geq V_{TO}, V_{DS}\geq 0\\ 0 & V_{GS}<V_{TO}, V_{DS}\geq 0\end{cases} \quad (1)$$

where β is the drain saturation current constant for V_{GS}=0, V_{TO} is the "Pinchoff" voltage, λ is the coefficient controlling the channel current increase with increasing drain-source voltage, and α is the coefficient controlling the slope of the channel current in the ohmic region.

Biasing the HEMT with $V_{GS}\cong V_{TO}$ and V_{DS} in the saturation region, $I_{DS}\cong\beta(V_{GS}-V_{TO})^2$ for $V_{GS}\geq V_{TO}$ and 0 for $V_{GS}<V_{TO}$, thus obtaining a truncated nonlinearity characteristic.

The NLC has also the input and output active stages as illustrated in Figure 2, where $HEMT_2$ is the transistor biased in the non-linear region as stated before. The input stage of the nonlinear circuit was implemented with a common-gate configuration, which provides a broadband input impedance matching (7), that can be electronically tuned to minimise the signal degradation due to the back reflections. For the output stage we have used a common-source transistor to obtain an output impedance matching at the data rate frequency.

At the input of the NLC, besides the common-gate, there is a by-pass capacitor that provides the necessary reshaping of the incoming signal, and therefore an additional prefilter at the NLC input is not necessary. This will be shown later in this paper, comparing the obtained jitter results to the presented in the literature, when using optimised prefilters.

In order to amplify the clock component generated by the NLC and to reduce the degradation caused by the spurious modes of the DR filter, we have implemented a bandpass amplifier centred at 20 GHz with a gain higher than 15 dB and a high out of band roll-off frequency response. The first step in the amplifier design was to build a single stage using a HEMT with appropriate size, suitable polarisation networks and input and output impedance matching networks, in order to simplify the project and simultaneously allow the maximum gain. To obtain the desired amplification level (>15 dB) we have cascaded three amplification stages.

Figure 3 *a)* shows the layout of the circuit, including the amplifier and the nonlinearity. To facilitate the electrical connection of the monolithic circuit to the NBPF, the NLC output and the amplifier input are in the same side of the circuit. In Figure 3 *b)* is presented the assembled circuit prototype.

EXPERIMENTAL RESULTS

The MMIC was mounted on a carrier and bond wires were used to connect it to the external circuits. The CRU measured impedance matching results are presented in Figure 4. The input matching is higher than 9 dB in a frequency range greater than 18 GHz, and the output matching is, at 20 GHz, approximately 12 dB. From these results we verify that the CRU presents the desired impedance matchings.

In Figure 5 are presented the spectra obtained at the output of the nonlinear circuit from a pseudo-random bit sequence (PRBS) at 19.90656 Gsymb/s (2*STM-64) when using binary NRZ and 4-level codings, where can be observed the generated discrete components at the data rate.

In Figure 6 *a)* is presented the amplifier frequency response (the gain is approximately 19 dB at 20 GHz). Figure 6 *b)* presents the cascaded amplifier and narrow bandpass filter frequency response. The NBPF used (8) has a quality factor close to 750, an insertion loss, including the SMA connectors, of 2.7 dB, and a phase slope of 4.4°/MHz.

Observing Figure 6 *b)* we verify that the NBPF spurious modes are completely attenuated and that the gain is perfectly tuned at the data rate, being at that frequency approximately 13.8 dB. From these results it can be concluded that only the component generated at the data rate by the NLC (see Figure 5) will be amplified, thus allowing for the clock signal recovery with proper power level and with low associated jitter.

PERFORMANCE ASSESSMENT

In this point is tested the efficiency of the CRU, consisting of the two implemented subsystems (NLC and amplifier) connected by a NBPF (8), to recover the clock signal from sequences with no power at the data rate.

Figure 7 presents the eye-diagrams of the recovered clock signals (bottom) and the input waveforms (up). These input waveforms are 19.90656 Gsymb/s PRBS of length 2^{31}-1 bits and amplitude 600 mV, with two different line codings, binary NRZ (Figure 7 *a)*) and 4-level (Figure 7 *b)*). The measured amplitude and jitter of the clock signal are respectively 200 mV and 0.010 UI RMS for the NRZ case, and 140 mV and 0.018 UI RMS for the 4-level case. As expected, considering the analysis presented by Franks and Bubrouski (2), the jitter values obtained when considering 4-level coding are higher than for the NRZ case.

The obtained jitter values are quite reasonable when compared to the ones presented in the literature, considering other approaches. For instances, in reference (9) it was obtained a jitter less than 0.04 UI RMS for 20 Gbit/s NRZ coding and considering a PRBS of length 2^{23}-1 bits, using a completely integrated open-loop CRU, with a fully-balanced narrowband regenerative frequency divider.

CONCLUSIONS

The designs and experimental characterisation of an unbalanced nonlinearity and a tuned amplifier to be used in an open-loop clock recovery unit at 20 Gsymb/s were presented. The built nonlinear circuit based on an unbalanced structure is a simple and low cost solution for very high bit rates. Another innovation of the presented nonlinearity is that its input stage provides the necessary formatting to the signal entering its squarer stage, thus avoiding the use of an additional prefilter. The obtained jitter performance of the CRU consisting of the two implemented subsystems, connected by an external high-Q bandpass filter (8), is quite acceptable when compared to other approaches presented in the literature (8)(9), making this approach adequate for building a simple, robust and easily manufacturable clock recovery unit.

ACKNOWLEDGEMENT

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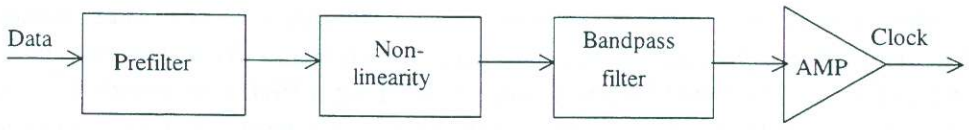


Figure 1 - Block diagram of an open-loop clock recovery circuit

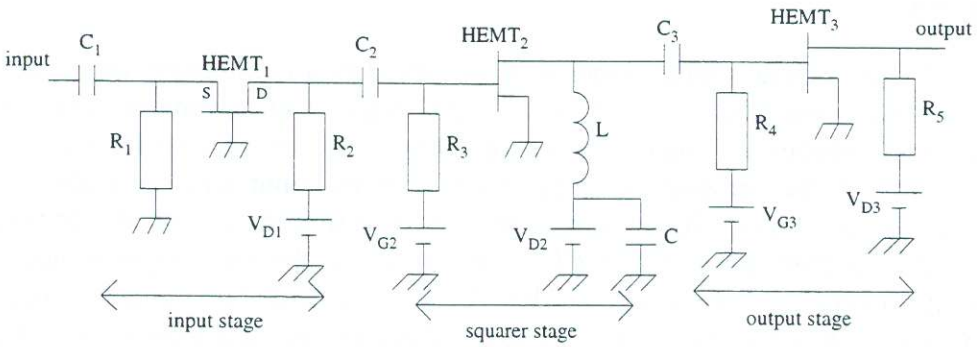


Figure 2 - Nonlinearity simplified electrical circuit

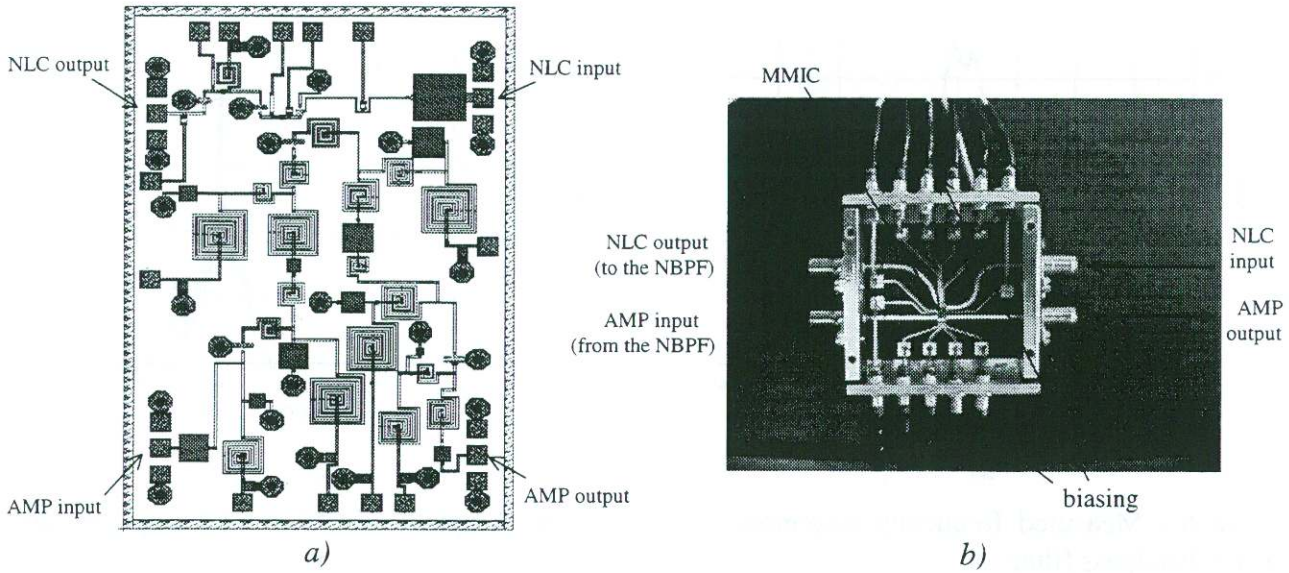


Figure 3 - *a)* Layout of the integrated circuit (nonlinear circuit and tuned amplifier, respectively at the top and bottom) submitted to the Foundry (2 mm x 3 mm). *b)* Assembled circuit prototype

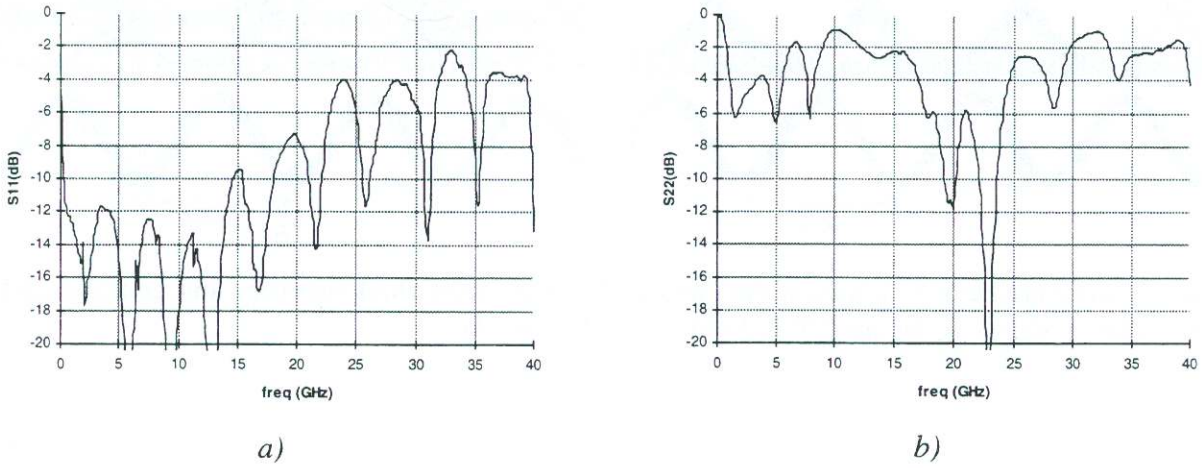


Figure 4 - The clock recovery unit measured matching results. *a)* Input matching ($20\log|S_{11}|$). *b)* Output matching ($20\log|S_{22}|$)

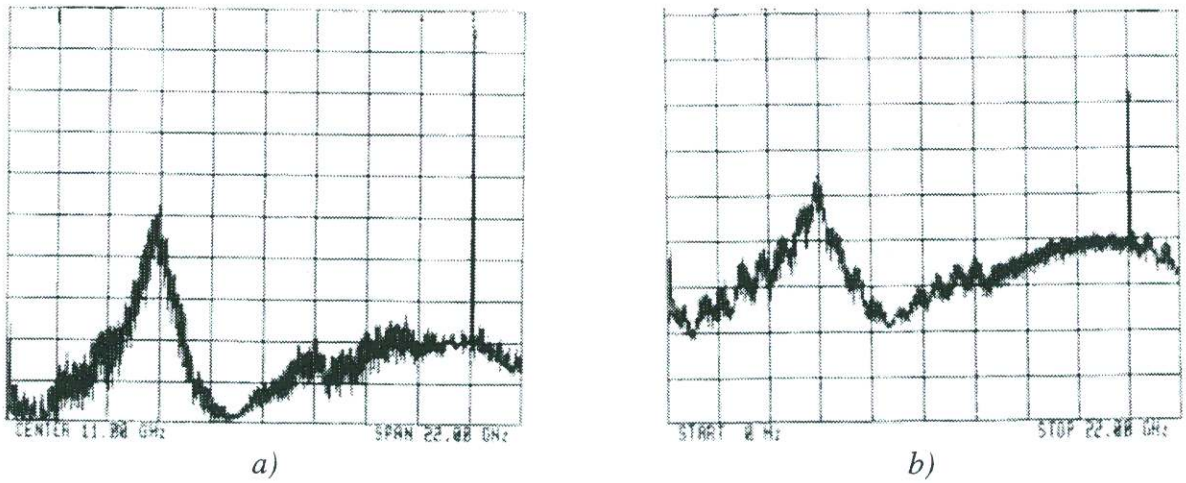
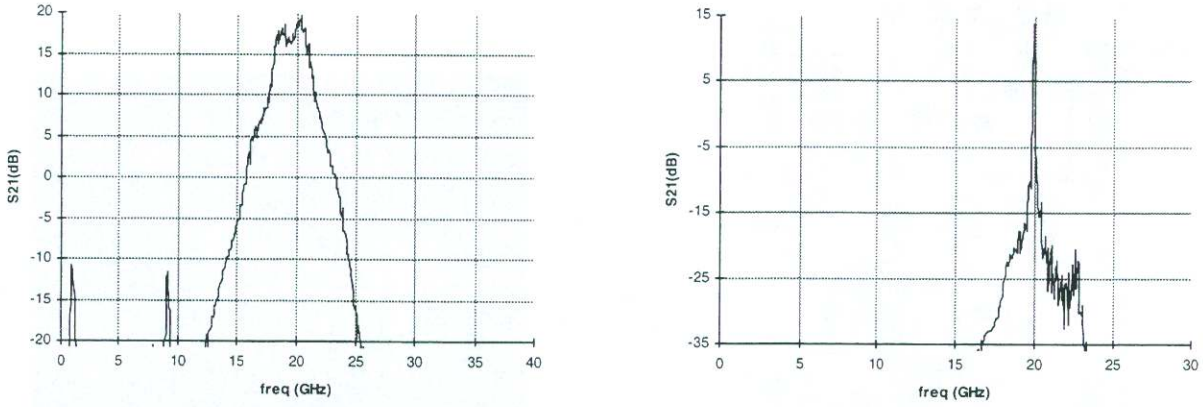
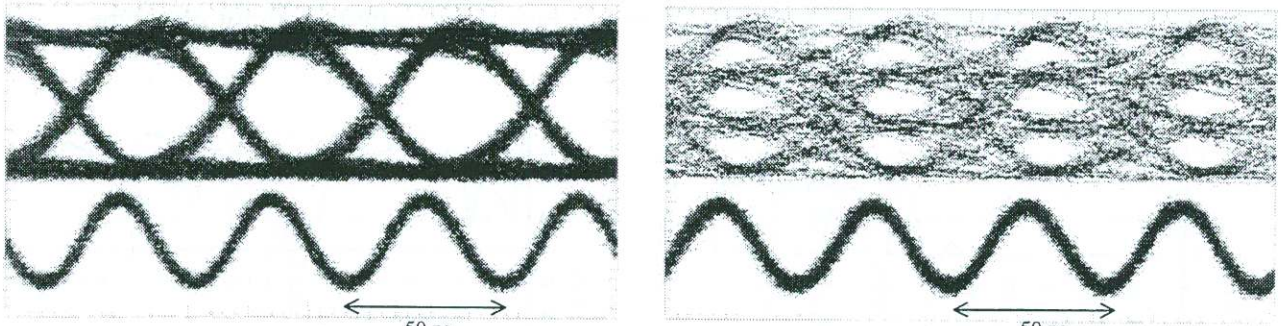


Figure 5 - Measured spectra at the output of the nonlinear circuit considering different line codings. *a)* NRZ (5 dB/div, -25.8 dBm at 19.90656 GHz). *b)* 4-level (10 dB/div, -29 dBm at 19.90656 GHz)



a) *b)*

Figure 6 - Measured frequency responses ($20\log|S_{21}|$). *a)* Amplifier. *b)* Cascaded amplifier and narrow bandpass filter



a) *b)*

Figure 7 - Measured eye-diagrams at the input and output of the clock recovery unit considering two different line codings. *a*) Binary NRZ. *b*) Multilevel (4-level)